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HDL LAB-10ECL48. VIVA - VOCE QUESTIONS Expand VHDL. What is the difference between VHDL and Verilog? What is the difference between (i) signal and variable (ii) generic & Parameter (iii) function & procedure (iv) task & function (v) always & initial (vi) register & variable (vii) signal & wire

HDL LAB VIVA VOCE Questions

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Viva Questions For Digital Electronics Lab

These questions are very useful as FPGA viva questions also. Question -1: Write a simple VHDL program for D Flipflop and D latch. Answer -1: Refer D Flipflop VHDL Code and D Latch VHDL Code Question -2: Write a VHDL program for 4X1 MUX(Multiplexer). Answer -2: Refer 4X1 MUX VHDL Program . Question -3: Write a VHDL code for 8 to 3 encoder.

10 VHDL,Verilog,FPGA interview questions and answers

Fundamentals of VLSI Lab viva and interview questions with answers for freshers.

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Question 1. What Is Vhdl? Answer : VHDL stands for "VHSIC Hardware Description Language." VHSIC, in turn, stands for "Very High Speed Integrated Circuit," which was a U.S. Department of Defense program. Question 2. What Can Be The Various Uses Of Vhdl? Answer : The VHDL language can be used for several goals like - To synthesize digital circuits.

VHDL Interview Questions & Answers - Wisdom Jobs

Course: 15EC53 - Verilog HDL Note: (i) Answer Five full questions selecting any one full question from each Module. (ii) Question on a topic of a Module may appear in either its 1st or 2nd question. Time: 3 Hrs Max. Marks: 80 Module-1 1 a. Explain a typical design flow for designing VLSI IC circuits using the block diagram. 08 b.

VERILOG HDL(15EC53) QUESTION BANK (Module 1 to Module 5)

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HDL Cholesterol - Lab Tests Online

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